SIES Graduate School of Technology

Department Of Electronics and Telecommunication Engineering

# Workshop on FPGA Design Using Verilog

**2nd January 2023 to 7th January 2023**

**Click here to register**

Since their introduction in the 1985, field programmable gate arrays (FPGAs) have become increasingly important to the electronics industry. They have the potential for higher performance and lower power consumption than microprocessors and compared with ASICs, offer lower non-recurrent engineering (NRE) costs, reduced development time, easier debugging and reduced risk. Since modern FPGAs can meet many of the performance requirements of ASICs, they are being increasingly used in their place. The aim of workshop is to provide a platform for students to learn, design and implement digital system on FPGA using Verilog/VHDL.

In this course students will learn Basics of FPGA Board , FPGA Programming using Verilog.

## About Instructors:

This course will be taught by a team of expert from SIESGST faculty-Electronics and Telecommunication Department, along with some Industry Experts.

**Faculty Members:**

1. Prof. Dr.Preeti Hemnani
2. Prof. Pranavi Nikam

## Course Objectives:

| |
|---|
| • To undersatnd FPGA and HDL language |
| • To understand design of combinational circuit using verilog |
| • To understand design of sequential circuit using verilog |
| • To understand Test bench and simulation uisng different tools |
| • To understand Finite state mahine design using verilog |
| • To undersatnd FPGA and HDL language |

## Course Outcomes:

At the end of the course, students will be able to

| |
|---|
| • Implement Verilog design using EDA and xilink platform |
| • Implement combinational circuits using Verilog |
| • Implement sequential circuits using Verilog |
| • Implement FSM using Verilog |
| • Implement hamming code , error detetction and correction using verilog |

## Course Content:

| Module | Contents | Hours |
|---|---|---|
| 1. | 1.1 Introduction to basics of FPGA<br>1.2 Introduction to Verilog coding: Data types,Constant, Parameters, Wires , Registers , operators<br>1.3 Continues and Procedural assignment statement | 5hrs |
| 2. | 2.1 Different Modeling style : Gate level, Structural level, Behavioral Level<br>2.2 Programming based on different modeling style<br>2.3 Xilink software introduction | 7hrs |
| 3. | 3.1: Implementation of combinational circuits on FPGA: Half adder , Full adder , Multiplexer, Decoder | 6hrs |
| 4 | 4.1 : Implementation of sequential circuits on FPGA<br>Flip Flop, Asynchronous counter, Synchronous counter, Mod counter , Sequence detector | 8 hrs |
| 5 | 5.1 : FSM design<br>5.2: FSM implementation on FPGA | 8hrs |
| 6 | Hamming code, Error detection and correction using Verilog on FPGA | 6 Hrs |
| 7 | Designing of Project. | 15hrs |

## Assessment:

1. Module wise assignments and quizzes will be taken.
2. Mini Projects will be assigned in a group of 4 students.

## Course Coordinators:

Dr. Preeti Hemnani

preetih@sies.edu.in

8169215360

Pranavi Nikam

pranavim@sies.edu.in

9870201503

SIES Graduate School of Technology
Sri Chandrasekarendra Saraswati Vidyapuram
Sector 5, Nerul, Navimumbai-400706

## Department of Electronics & Telecommunication Engineering

# Event Report

## FPGA Design using Verilog
**(2/1/2023 to 7/1/2023)**

| Event Information |
|---|
| **Event Type:** Student Development program with Intenship |
| **Event title**: FPGA Design using Verilog |
| **Resource Person:** Dr.Preeti Hemnani , Prof. Pranavi Nikam |
| **Event date:2/1/2023 to 7/1/2023** |
| **Organized for:**Student Faculty - |
| **Organizedby** Department : Electronics & Telecommunication Engineering |
| **Target audience :TE students**<br>**Branch: EXTC / CE**<br>**Number of students registered:30**<br>**Number of students joined on first day:18**<br>**Number of students completed the course:18**<br>**Number of students completed the internship projects:18** |
| **Attachments: 1. List of students with internship Projects completed by the students**<br><br>**2. Attendance report** |

**3. Feedback**

**4. Certificate, Photographs (in JPEG/PNG)**

## Event Description

EXTC department faculties have conducted 15 days student development program followed by internship, “FPGA Design using Verilog”. Program was conducted by Prof. Pranavi Nikam and Prof. Dr. Preeti Hemnani.

Objective of the workshop was to bridge the gap between industry requirements and academic. 18 students attended the course and successfully developed and submitted project individually. Students completed their projects during online internship by SIESGST.

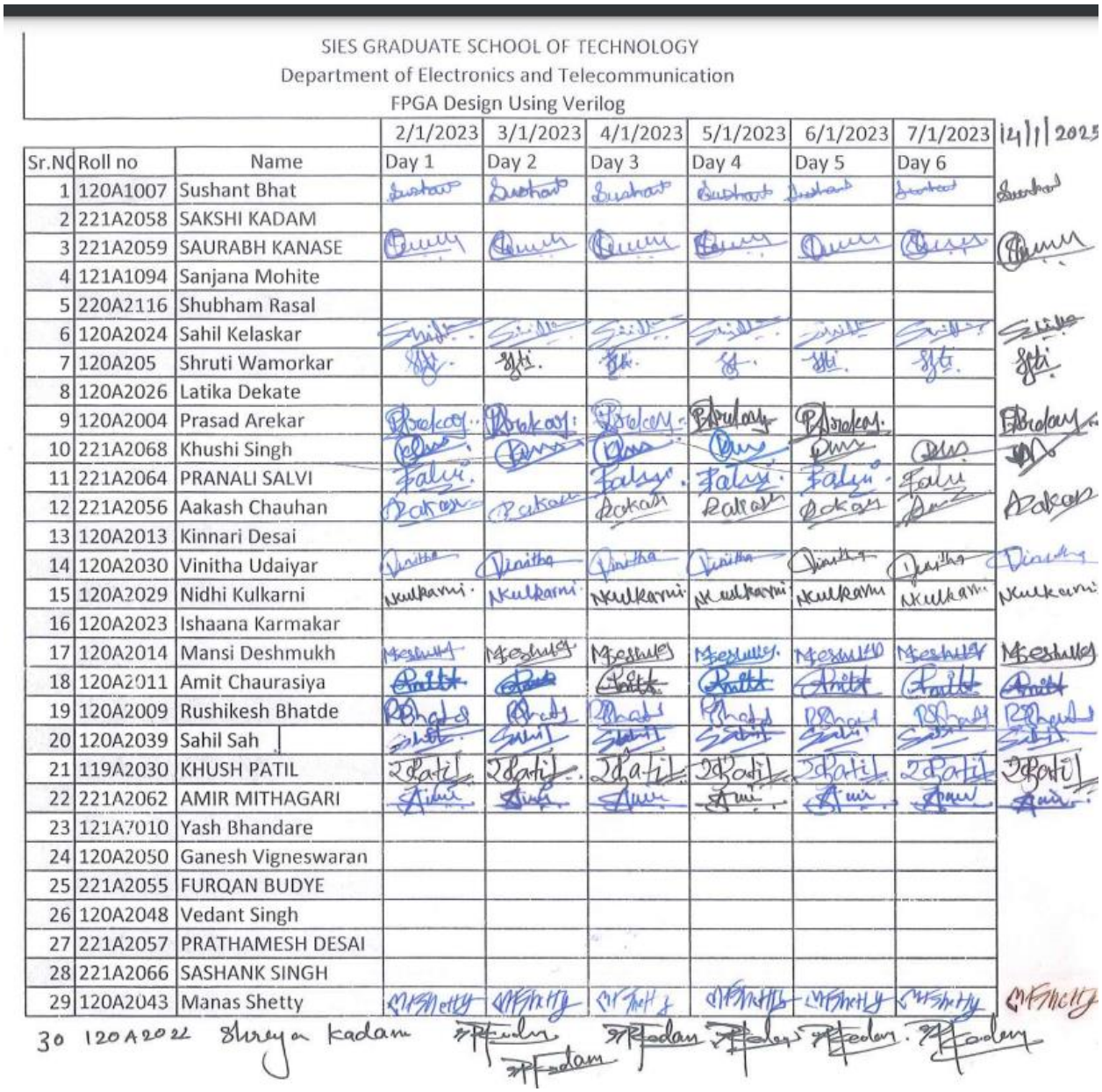
Certificates were given to students on successful completion and presentation of developed applications. Feedback was collected and overall feedback shows students were satisfied with content.

### 1. List of Students :

| STUDENT NAME | CLASS-DEPARTMENT (E.G. SE-ECS) | PROJECT TITLE |
|---|---|---|
| Sushant Ramesh Bhat | TE-CE | Design of Comparator and implementation on FPGA |
| Saurabh Dhanaji Kanase | TE-EXTC | Design of priority encoder with seven segment and implementaion on FPGA |
| Sahil Kelaskar | TE-EXTC | Implementation of BCD counter with seven segment on FPGA |
| Shruti Madhav wamorkar | TE-EXTC | Implementation of BCD counter with seven segment on FPGA |
| Prasad Arekar | TE-EXTC | Implementation of BCD counter with seven segment on FPGA |
| Khushi singh | TE-EXTC | Design of multiplexer and implemention on FPGA |
| Pranali salvi | TE-EXTC | Design of multiplexer and implemention on FPGA |
| Aakash chauhan | TE-EXTC | Design of multiplexer and implemention on FPGA |
| Vinitha Rajavelu udaiyar | TE-EXTC | Design of Demultiplexer and Implementation on FPGA. |
| Nidhi Kulkarni | TE-EXTC | Design of Demultiplexer and Implementation on FPGA. |
| Mansi Deshmukh | TE-EXTC | Implementation of Elevator controller on FPGA |
| Amit Chaurasiya | TE-EXTC | Implementation of Elevator controller on FPGA |
| Rushikesh Bhatde | TE-EXTC | Design of priority encoder with seven segment and implementaion on FPGA |
| Sahil Santosh Sah | TE-EXTC | Implementation of BCD counter with seven segment on FPGA |

| | | |
|---|---|---|
| **Khush Vasudeo Patil** | **BE-EXTC** | **Design of Comparator and implementation on FPGA** |
| **Amit Mithagiri** | **TE-EXTC** | **Design of priority encoder with seven segment and implementaion on FPGA** |
| **Manas shetty** | **TE-EXTC** | **Design of Comparator and implementation on FPGA** |
| **Shreya Kadam** | **TE-EXTC** | **Design of Demultiplexer and Implementation on FPGA.** |

## 2. Attendance report :



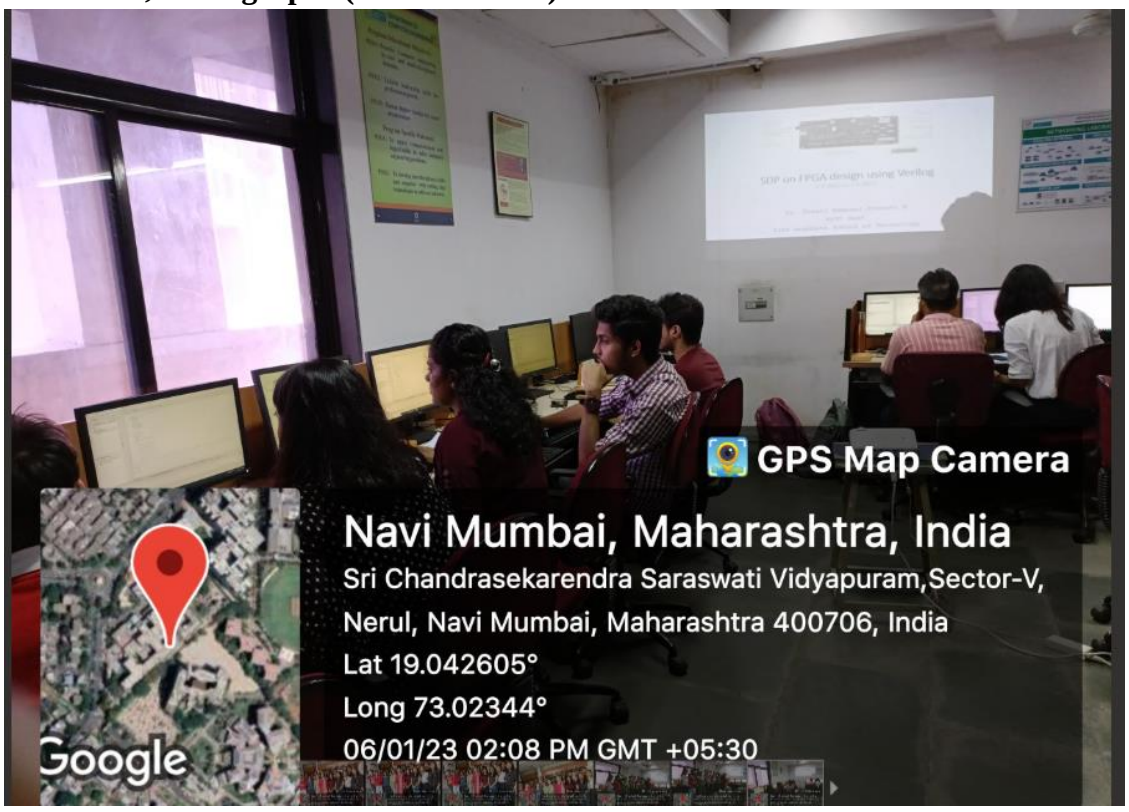
SIES GRADUATE SCHOOL OF TECHNOLOGY
Department of Electronics and Telecommunication
FPGA Design Using Verilog

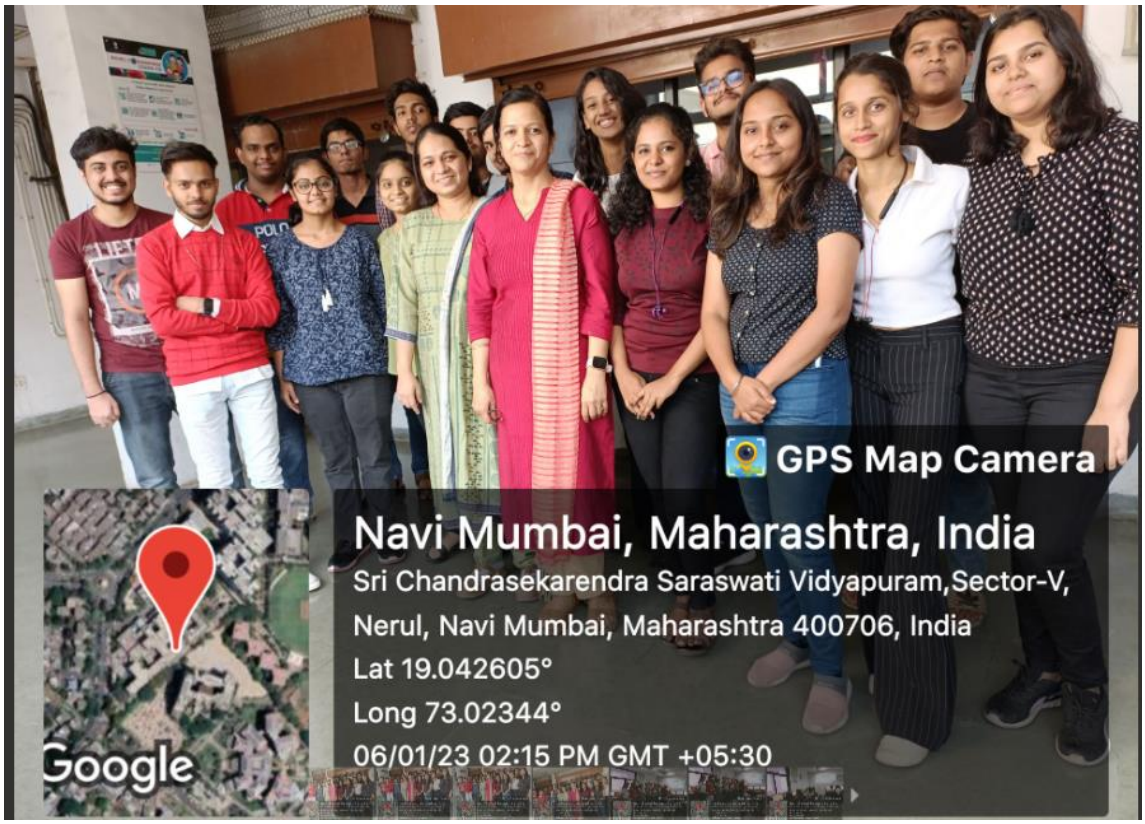
| Sr.NO | Roll no | Name | 2/1/2023 Day 1 | 3/1/2023 Day 2 | 4/1/2023 Day 3 | 5/1/2023 Day 4 | 6/1/2023 Day 5 | 7/1/2023 Day 6 | 14/1/2023 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 120A1007 | Sushant Bhat | | | | | | | |
| 2 | 221A2058 | SAKSHI KADAM | | | | | | | |
| 3 | 221A2059 | SAURABH KANASE | | | | | | | |
| 4 | 121A1094 | Sanjana Mohite | | | | | | | |
| 5 | 220A2116 | Shubham Rasal | | | | | | | |
| 6 | 120A2024 | Sahil Kelaskar | | | | | | | |
| 7 | 120A205 | Shruti Wamorkar | | | | | | | |
| 8 | 120A2026 | Latika Dekate | | | | | | | |
| 9 | 120A2004 | Prasad Arekar | | | | | | | |
| 10 | 221A2068 | Khushi Singh | | | | | | | |
| 11 | 221A2064 | PRANALI SALVI | | | | | | | |
| 12 | 221A2056 | Aakash Chauhan | | | | | | | |
| 13 | 120A2013 | Kinnari Desai | | | | | | | |
| 14 | 120A2030 | Vinitha Udaiyar | | | | | | | |
| 15 | 120A2029 | Nidhi Kulkarni | | | | | | | |
| 16 | 120A2023 | Ishaana Karmakar | | | | | | | |
| 17 | 120A2014 | Mansi Deshmukh | | | | | | | |
| 18 | 120A2011 | Amit Chaurasiya | | | | | | | |
| 19 | 120A2009 | Rushikesh Bhatde | | | | | | | |
| 20 | 120A2039 | Sahil Sah | | | | | | | |
| 21 | 119A2030 | KHUSH PATIL | | | | | | | |
| 22 | 221A2062 | AMIR MITHAGARI | | | | | | | |
| 23 | 121A7010 | Yash Bhandare | | | | | | | |
| 24 | 120A2050 | Ganesh Vigneswaran | | | | | | | |
| 25 | 221A2055 | FURQAN BUDYE | | | | | | | |
| 26 | 120A2048 | Vedant Singh | | | | | | | |
| 27 | 221A2057 | PRATHAMESH DESAI | | | | | | | |
| 28 | 221A2066 | SASHANK SINGH | | | | | | | |
| 29 | 120A2043 | Manas Shetty | | | | | | | |
| 30 | 120A2022 | Shreya Kadam | | | | | | | |

## 3. Feedback

| ID | Name | Roll NO | Full Name ( will be p | Branch | are you able to understand basic of FPGA and Verilog Coding ? | Are you able to understand combinational circuit executior | Are you able to understand Sequential circuit execution? | Are you able to understand FSM execution ? | Content Delivery by Speakers | How relevant you think it was for your future | Effectiveness of SDP | Satisfaction in general | Any other suggestion or Your views about SDP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Shruti Wamorkar | 120A2052 | Shruti Madhav Wamorkar | EXTC | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | Very interactive |
| 2 | Khushi Singh | 221A2068 | SINGH KHUSHI RAJIV | EXTC | 5 | 4 | 5 | 4 | 5 | 5 | 4 | 5 | Overall the session was good |
| 3 | Aakash Chauhan | 221A2056 | Aakash chauhan | EXTC | 4 | 5 | 4 | 5 | 5 | 5 | 4 | 4 | No suggestion |
| 4 | Shreya Kadam | 120A2022 | Shreya Kadam | EXTC | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | . |
| 5 | Rushikesh Bhatde | 120A2009 | Rushikesh Uday Bhatde | EXTC | 2 | 3 | 3 | 3 | 3 | 3 | 2 | 4 | Proper faculty is needed to teach Verilog. |
| 6 | Manas Shetty | 120A2043 | Shetty Manas Taranath | EXTC | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | |
| 7 | Vinitha Udaiyar | 120A2030 | Vinitha Rajavelu Udaiyar | EXTC | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | Add on Sdp related to data science concepts |
| 8 | SAURABH KANASE | 221A2059 | Saurabh Dhanaji Kanase | EXTC | 5 | 4 | 4 | 5 | 5 | 4 | 4 | 5 | Nothing |
| 9 | Amit Chaurasiya | 120A2011 | Chaurasiya Amit Dharmendra | EXTC | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | It was very good, good explanation done by the speaker ☺🅱☺🅱, ek dum se hi maza aa gaya |
| 10 | Mansi Deshmukh | 120A2014 | Mansi S. Deshmukh | EXTC | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | --- |
| 11 | PRANALI SALVI | 221A2064 | Pranali Salvi | EXTC | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | No |
| 12 | Prasad Arekar | 120A2004 | Prasad Vishwas Arekar | EXTC | 4 | 3 | 4 | 3 | 5 | 5 | 5 | 5 | Nil |
| 13 | Sahil Kelaskar | 120A2024 | Sahil Hemant Kelaskar | EXTC | 4 | 4 | 3 | 4 | 4 | 4 | 5 | 5 | . |
| 14 | KHUSH PATIL | 119A2030 | Khush Vasudeo Patil | EXTC | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | NA |
| 15 | Sushant Bhat | 120A1007 | Sushant Bhat | CE | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | Nothing |

4. **Certificate, Photographs (in JPEG/PNG) :**






Quiz Result:

**Operator which precedes the operand** (1 point)

87% of respondents (13 of 15) answered this question correctly.

More Details  Insights

| | | |
|---|---|---|
| Unary | 13 | ✓ |
| Binary | 1 | |
| Ternary | 0 | |
| None | 1 | |

**#40 $finish indicates** (1 point)

80% of respondents (12 of 15) answered this question correctly.

More Details  Insights

| | | |
|---|---|---|
| end of simulation time | 0 | |
| end of simulation at 40 time units | 12 | ✓ |
| suspend simulation at 40 time u... | 3 | |
| None | 0 | |

**What is the time period of clock #10 clock = ~clock** (1 point)

67% of respondents (10 of 15) answered this question correctly.

More Details  Insights

| | | |
|---|---|---|
| 10 | 5 | |
| 20 | 10 | ✓ |
| 5 | 0 | |
| 10 | 5 | |

Certificate :

SIES Graduate School of Technology
RISE WITH EDUCATION

# CERTIFICATE
## OF COMPLETION

CR No. EXTC/SDP/0123/450

this is to certify that

**Amit Chaurasiya**

has successfully completed the value-added course on
**FPGA Design Using Verilog,**
followed by fifteen days of in-house internship,
from 2nd Jan, 2023 to 14th Jan, 2023,
organized by **Electronics and Telecommunication** department, SIES GST.
During the internship, he/she has successfully completed the project titled,
**Implementation of Elevator controller on FPGA**

Prof. Pranavi Nikam — Dr.Preeti Hemnani — Dr. Atul Kemkar